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New Cascaded Multilevel Inverter Topology with Reduced Number of Switches

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Abstract: Demand for high-voltage and high power inverters are increasing day by day. Thus multilevel inverter topologies are becoming more popular. In this paper a multilevel inverter topology is discussed. The inverter consists of series connection of a number of basic units. Cascaded multilevel inverter topology can be symmetric or asymmetric. The adopted basic unit generates positive voltage levels and negative voltage levels can be obtained by adding a H-bridge. Since the number of switches used to generate a particular number of voltage levels is less compared to the conventional topologies, cost and the installation space reduces. Four different algorithms are also discussed to generate even and odd number of voltage levels. The features of the inverter can be verified using the MATLAB simulation.

Keywords: Asymmetric, basic unit, cascaded multilevel inverter, H-bridge, symmetric.

I. INTRODUCTION

Multilevel inverters are becoming recent trends, because of its modularity and simplicity of control to generate particular number of levels. Multilevel inverters have a number of applications such as UPS, in power grid, as solar inverter, induction heating and number of other applications. By increasing the number of dc voltage sources, a sinusoidal like waveform can be generated. Thus the total harmonic distortions decreases which has a great significance in power grid applications. A sine wave output is desirable because many electrical products are engineered to work best with a sine wave AC power source. The standard electric utility power attempts to provide a power source that is a good approximation of a sine wave.

Sine wave inverters with more than three steps in the wave output are more complex and have significantly higher cost than a modified sine wave, with only three steps, or square wave (one step) types of the same power handling. Switch-mode power supply (SMPS) devices, such as personal computers function on quality of sine wave power. AC motors directly operated on non-sinusoidal power may produce extra heat, may have different speed-torque characteristics, or may produce more audible noise than when running on sinusoidal power thus the multilevel inverters with reduced number of switches becomes more significant.

The multilevel inverters is classified as, neutral point clamped inverters, flying capacitor multilevel inverters and cascade multilevel inverters [1]-[3]. Of this three category cascaded multilevel inverter is recent trend because of its reliability. Cascaded multi level inverter uses reduced number of power switches and it produces a sinusoidal like waveform. [4],[5],[6]. Cascaded multilevel inverter is series connection of power switches and dc voltage sources. Cascaded multilevel inverters have several advantages when compared to other topologies. The main advantages of using the cascaded multilevel inverters are the high power quality waveforms due to the reduction in the total harmonic distortion and also the reduction of dv/dt stresses on the load, Cascaded multilevel inverters can be classified as symmetric and asymmetric multilevel inverters. The main difference between symmetric and asymmetric configuration is the magnitude of dc sources. In symmetric configuration magnitudes of dc sources are same, whereas in the asymmetric configuration magnitudes of the dc sources are different [7]. By using the cascaded multilevel inverters desired number of output voltage levels can be obtained by series connection of a number of dc voltage sources. A number of different topologies have been presented in the literature. Numerous basic units are also presented in the literature. The disadvantage of the symmetric configuration is that it requires more number of power switches when compared to the asymmetric configurations. A large number of asymmetric configurations are also present in literature.[7], [8], [9] and [10].Bt the dc voltage magnitude is very high in these papers. Single phase and three phase multilevel inverters can be produced by the series connection of a large number of the basic units. By using the same topology with the same number of switches different number of voltage level can be obtained by implementing different algorithms. In each algorithm the magnitude of the dc voltage sources are different. It can be symmetric or asymmetric

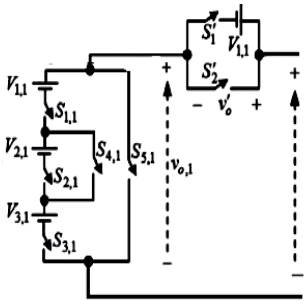

Fig.1. Basic unit

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TABLE I PERMITTED TURN ON AND TURN OFF OF THE BASIC UNIT

State	Switch states							v_o
	S_1'	S_2'	$S_{1,1}$	$S_{2,1}$	$S_{3,1}$	$S_{4,1}$	$S_{5,1}$	
1	off	on	off	off	off	off	On	0
2	on	off	off	off	off	off	On	$V_{1,1}$
3	off	on	on	off	on	on	Off	$V_{1,1}$+ $V_{2,1}$
4	on	on	on	on	on	off	Off	$V_{1,1}$+ $V_{2,1}$+ $V_{3,1}$
5	on	off	on	on	on	off	Off	$V_{1,1}$ +$V_{1,1}$ + $V_{2,1}$+ $V_{3,1}$

To increase the output voltage levels with a reduced number of power switches a new basic unit is presented in this paper. The basic unit is able to generate only positive voltage levels. The negative voltage levels can be obtained by adding an H-bridge. By the addition of required number of basic units number of voltage levels can be increased. Fig.1. shows the adopted basic unit. The switches S_1' and S_2' are used to generate the voltage $V_{1,1}$. All other voltage levels can be obtained by the basic unit.

II. CASCADED MULTILEVEL INVERTER TOPOLOGY

Cascade multilevel inverters have been developed for electric utility applications. It consists of series connection of a number of basic units. Cascaded multilevel inverter can be designed as single phase cascaded multilevel inverters and three phase cascaded multilevel inverters depending on the applications. Fig.2 represents single phase cascaded multilevel inverter with the new basic unit. This can be symmetric multilevel inverter or asymmetric multilevel inverter with the same number of switches only by varying the magnitude of dc voltage sources.

Here n number of basic units can be connected in series to generate a large number of voltage levels. Thus the output voltage is the sum of the output voltages of individual basic units and v_0'. It can be represented as follows,

$$v_0' = v_{0,1}(t) + v_{0,2}(t) + \ldots\ldots\ldots + v_{0,n}(t) + v_0'(t) \qquad (1)$$

The number of switches and number of sources can be obtained by the following equation,

$$N_{switch} = 5n+(2) \qquad (2)$$

$$N_{source} = 3n+1 \qquad (3)$$

Where n is the number of series connected basic units.

The cost of an inverter mainly depends on the maximum amount of blocked voltage by the switches. Here the blocked voltage by the switches decides the voltage rating of the switches. The values of blocked voltages of switch can be given as,

$$V_{S'1} = V_{S'2} = V_{1,1} \qquad (4)$$

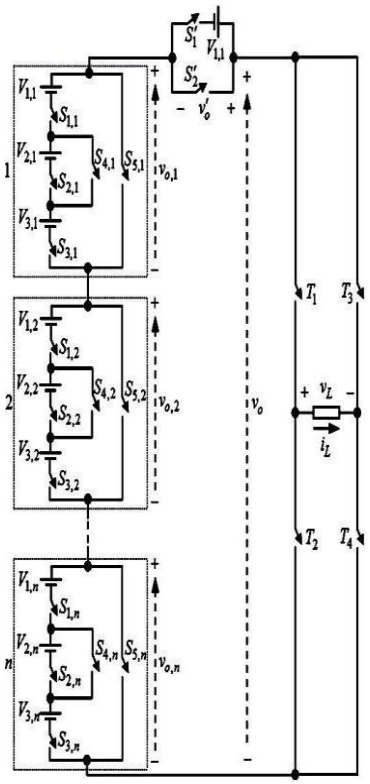

Fig.2. Single phase cascaded multilevel inverter topology

$$V_{S1,j} = V_{S3,j} = \frac{V_{1,j}+V_{2,j}+V_{3,j}}{2} \qquad (5)$$

$$V_{S1,j} = V_{S2,j} = V_{2,j} \qquad (6)$$

$$V_{S5,j} = V_{1,j} + V_{2,j} + V_{3,j} \qquad (7)$$

$$V_{T1} = V_{T2} = V_{T3} = V_{T4} = V_{o,max} \qquad (8)$$

Where j= 1, 2, … …n

Cascaded three phase inverters have a numerous applications, especially in power grid applications. By connecting n number of basic units in each phase three phase's cascaded multilevel inverter can be formed. The H-bridge used for inverting the output of the basic unit can be used common in each phase. Hence the voltage levels can be increased by connecting the large number of basic units. Fig.3. shows three phases cascaded multilevel inverter with the adopted basic unit.

III. ALGORITHMS

Different algorithms can be used for the same basic unit for which the number of voltage levels and other parameters are different. Four different algorithms are adopted in which one of them is symmetric algorithm and the rest of them is asymmetric algorithms.

i. Symmetric Algorithm

First algorithm is a symmetric algorithm in which the magnitudes of the dc sources are same. Magnitudes of the dc voltage sources can be given as,

$$V_{1,j} = V_{2,j} = V_{3,j} = V_{dc} \qquad (9)$$

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for j= 1, 2,……, n

The number of levels that can be obtained using the first algorithm is given by,

$$N_{level} = 6n + 3 \quad (10)$$

The maximum output voltage obtained while implementing the first algorithm is given by,

$$V_{O,max} = (3n + 1)V_{dc} \quad (11)$$

Blocking voltage is given by,

$$V_{block} = (21n + 6)V_{dc} \quad (12)$$

ii. Asymmetric Algorithm Type I

Second algorithm is an asymmetric algorithm in which the magnitudes of the dc voltage sources are different. It can be given as,

$$V_{1,1} = V_{2,1} = V_{3,1} = V_{dc} \quad (13)$$

$$V_{1,j} = V_{2,j} = V_{3,j} = 2V_{dc} \quad (14)$$

for j= 2, 3,……, n

The number of voltage levels can be given as,

$$N_{level} = 12n - 3 \quad (15)$$

The maximum output voltage obtained while implementing the first algorithm is given by,

$$V_{O,max} = (6n - 2)\, V_{dc} \quad (16)$$

Blocking voltage is given by,

$$V_{block} = (40n - 13)V_{dc} \quad (17)$$

iii. Asymmetric Algorithm Type II

The third algorithm is an asymmetric algorithm. The magnitudes of dc voltage sources can be given as,

$$V_{1,1} = V_{2,1} = V_{3,1} = V_{dc} \quad (18)$$

$$V_{1,j} = \frac{1}{3}V_{2,j} = V_{3,j} = 3^{j-2}\, V_{dc} \quad (19)$$

for j= 2, 3,……, n

The number of voltage levels can be given as,

$$N_{level} = 5(3^{n-1}) + 4 \quad (20)$$

The maximum output voltage can be given as,

$$V_{O,max} = \frac{5(3^{n-1}+3)}{2} V_{dc} \quad (21)$$

Blocking voltage is given by,

$$V_{block} = [82(3^{n-1}) - 7]\, V_{dc} \quad (22)$$

iv. Asymmetric Algorithm Type III

Fourth algorithm is an asymmetric algorithm. The magnitude of dc voltage sources can be given as,

$$V_{1,j} = 0.5V_{2,j} = V_{3,j} = 2^{j-1}\, V_{dc} \quad (23)$$

for j= 1, 2,……, n

The number of voltage levels can be given as,

$$N_{level} = 2^{n+3} - 5 \quad (24)$$

The maximum output voltage can be given as,

$$V_{O,max} = (2^{n+2} - 3)V_{dc} \quad (25)$$

Blocking voltage is given by,

$$V_{block} = [7(2^{n+2}) - 22]\, V_{dc} \quad (26)$$

IV. SIMULATION RESULTS

Simulation of the multilevel inverters can be done using MATLAB SIMULINK. The magnitude of the dc voltage sources are the same while using the first algorithm. Fig.3. shows the MATLAB Simulink model of single phase multilevel inverter. Four algorithms can be simulated using same number of switches and by changing the switching pattern. Fig.4. shows the MATLAB Simulink model of three phase multilevel inverter. Each phase represents a single phase cascaded multilevel topology. In each phase n number of basic units is connecter in series. Resistive Inductive load is connected in each case. The output voltages of cascaded multilevel inverter with different algorithms are shown in Fig. 5. Here the number of basic units taken is two.

The maximum output voltages and the number of voltage levels will be different in each algorithms. The best performance can be obtained if using an asymmetrical configuration. Of the four algorithms first algorithm is the algorithm for the symmetric configuration. The remaining three are for asymmetric configuration. For n=2 and V_{dc} =20V the amplitude of the output voltage when Symmetric algorithm is implemented is about 140V and the number of levels is 15. With same number of basic units the amplitude of output voltage using the Asymmetric algorithm Type I is 200 V and the number of voltage levels is about 21.

The amplitude of output voltage when Asymmetric algorithm Type II is implemented is 180 V and the number of output voltage levels is 19 and when implementing Asymmetric algorithm Type III is 260 V and 27 levels. The switching pulses for the switches S1'and S2' is given in Fig. 5. From this its clear that fourth algorithm has the best performance among the three algorithms. The output voltage waveforms are given in Fig. 6. Three phase output voltage is generated by giving 120^0 phase shift.

Three phase circuit is done by using symmetric configuration. Phase delay can be given using the delay block in the Simulink. When analyzing the total harmonic distortion (THD) it is seen that THD is very less when compared to the conventional topologies. THD can be again reduced by increasing the number of basic units and using the asymmetric configuration. This cascaded topology uses reduced number of switches compared to conventional topologies to produce a particular voltage level. Hence the cost for the driver circuit can also be reduced by using this topology. By using the fourth algorithm the number of output voltage level can be increased to maximum.

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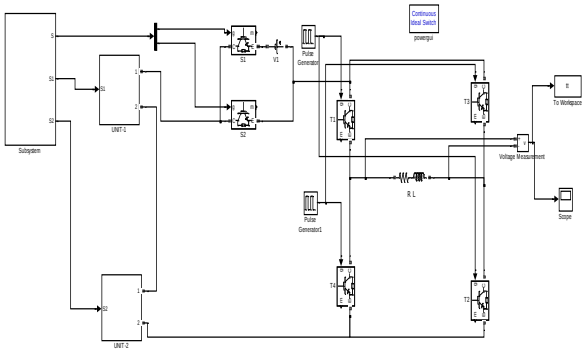


Fig.3. MATLAB SIMULINK model of single phase cascaded multilevel inverter

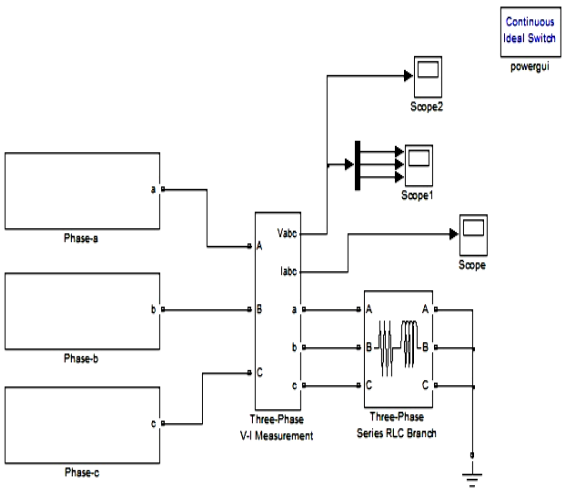


Fig.4. MATLAB SIMULINK model of three phase cascaded multilevel Inverter

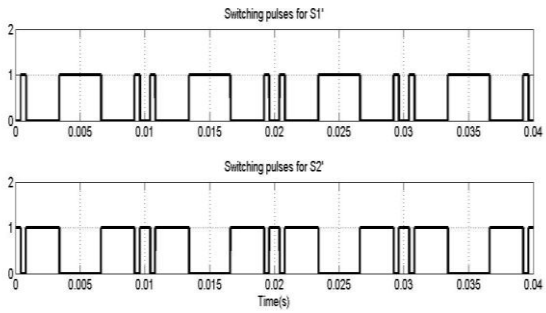
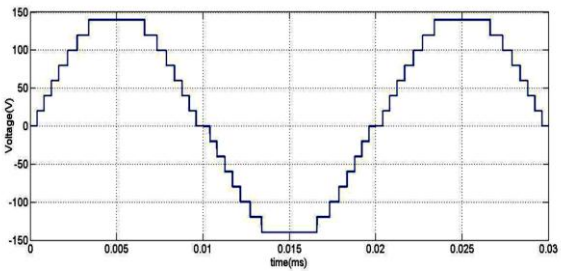
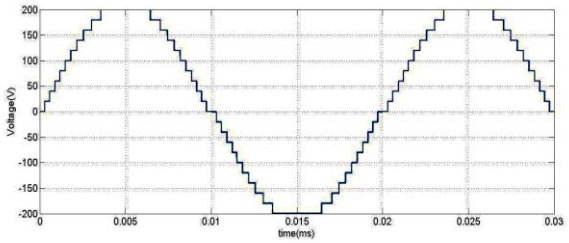


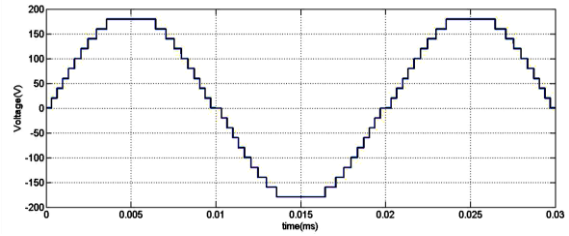
Fig.5. Switching pulses for S_1' and S_2' of three phase cascaded multilevel Inverter



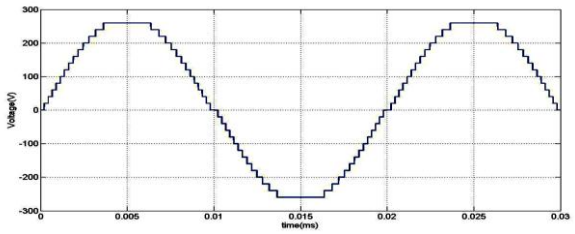
(a)



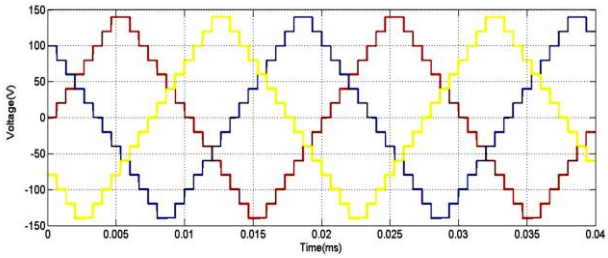
(b)



(c)



(d)



(e)

Fig.6. Output voltage waveforms. (a) First algorithm, (b) Second algorithm, (c) Third algorithm, (d) Fourth algorithm, (e) Three phase output voltage for symmetric configuration.

A comparative study of THD is shown in the Table II. By comparing the values of THD obtained, the fourth algorithm shows the minimum values of THD compared to the other algorithms.

TABLE II THD COMPARISON FOR DIFFERENT ALGORITHMS

Algorithms	No. of Levels	THD
Symmetric Algorithm	15	4.30%
Asymmetric Algorithm Type I	21	2.96%
Asymmetric Algorithm Type II	19	3.34%
Asymmetric Algorithm Type III	27	2.26%

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V. CONCLUSION

In this paper a new basic unit is presented. Here the series connection of a large number of basic unit a large number of output voltage levels can be generated. Increase in the number of levels results in a sinusoidal waveform. And as a result the total harmonic distortion decreases. Even and odd number of voltage levels can be generated using four different algorithms. The fourth algorithm shows best performance with maximum number of output voltage levels with the same number of power switches as used in the first, second and the third algorithms. This cascaded topology requires reduced number of power switches and driver circuits when compared to the conventional topologies.

REFERENCES

[1] A. A. Boora, A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "Voltage sharing converter to supply single-phase asymmetric four-level diode clamped inverter with high power factor loads," IEEE Trans. Power Electron., vol. 25, no. 10, pp. 2507–2520, Oct. 2010.

[2] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on natural point clamped inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[3] E. Babaei, M. F. Kangarlu, M. Sabahi, and M. R. Alizadeh Pahlavani, "Cascaded multilevel inverter using sub-multilevel cells," Electr. Power Syst. Res., vol. 96, pp. 101–110, Mar. 2013.

[4] E. Babaei, S. Alilu, and S. Laali, "A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge," IEEE Trans. Ind. Electron., vol. 61, no. 8, pp. 3932–3939,Aug. 2014.

[5] N. Farokhnia, S. H. Fathi, N. Yousefpoor, and M. K. Bakhshizadeh, "Minimizations of total harmonic distortion in a cascaded multilevel inverter by regulating of voltages DC sources," IET Power Electron., vol. 5, no. 1, pp. 106–114, Jan. 2012.

[6] S. Laali, K. Abbaszadeh, and H. Lesani, "Control of asymmetric cascaded multilevel inverters based on charge balance control methods," Int. Rev. Elect. Eng., vol. 6, no. 2, pp. 522–528, Mar./Apr. 2011.

[7] E. Babaei and S. H. Hosseini, "Charge balance control methods for asymmetrical cascade multilevel converters," in Proc. ICEMS, Seoul, Korea, 2007, pp. 74–79.

[8] M. Manjrekar and T. A. Lipo, "A hybrid multilevel inverter topology for drive application," in Proc. APEC, 1998, pp. 523–529.

[9] E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. Tarafdar Haque, and M. Sabahi, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology," Elect. Power Syst. Res., vol. 77, no. 8, pp. 1073–1085, Jun. 2007.

[10] S. Laali, K. Abbaszades, and H. Lesani, "A new algorithm to determine the magnitudes of DC voltage sources in asymmetrical cascaded multilevel converters capable of using charge balance control methods," in Proc. ICEMS, Incheon, Korea, 2010, pp. 56–61.